## AMENDMENTS TO THE CLAIMS

Please make the following amendments to the claims:

1. (Currently Amended) An interleaved generalized convolutional encoder, comprising:

~~(a)~~ a node, the node being capable of receiving a data input, the data input being a portion of ~~a data symbol~~ one of a stream of data symbols;

~~(b)~~ a memory element, the memory element being capable of storing a plurality of prior data inputs~~, the prior data inputs being a portion of each of a plurality of prior data symbols,~~ and outputting the plurality of prior data inputs after ~~being subjected to~~ a ~~variable~~ time delay having a value M, where M is configurable at run-time to a first value; and

~~(c)~~ a plurality of logic calculators,

~~(i) a portion of the plurality of logic calculators being capable of receiving a coefficient input,~~

~~(ii) the plurality of logic calculators including one or more final logic calculators, the one or more final logic calculators being capable of generating an output,~~

~~(A)~~ the plurality of logic calculators generating an output ~~being~~ based on the data input, the plurality of prior data inputs, the plurality of logic calculators, ~~the coefficient input,~~ and the ~~variable~~ time delay.

2. (Original) The encoder of claim 1, wherein the data input is a portion of a PAM symbol.

3. (Original) The encoder of claim 1, wherein the data input is processed by a serial to parallel converter prior to entering the encoder.

4. (Original) The encoder of claim 1, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

5. (Currently Amended) The encoder of claim 1, wherein the ~~variable~~ time delay is a plurality of unit time delays.

6. (Currently Amended) The encoder of claim 1, wherein a receiver sets the ~~variable~~ time delay.

7. (Currently Amended) The encoder of claim 1, wherein a receiver dynamically sets the ~~variable~~ time delay.

8. (Currently Amended) The encoder of claim 7, wherein the ~~variable~~ time delay is based on the quality of a transmission path between a transmitter and the receiver.

9. (Currently Amended) The encoder of claim 7, wherein the ~~variable~~ time delay is based on noise affecting the transmission of data between a DTE and the receiver.

10. (Currently Amended) The encoder of claim 1, wherein the ~~variable~~ time delay is three bauds.

11. (Original) The encoder of claim 1, wherein the plurality of logic calculators includes a plurality of binary exclusive-OR gates and a plurality of binary AND gates.

12. (Original) The encoder of claim 1, wherein the output is processed by a mapper after exiting the encoder.

13. (Original) The encoder of claim 1, wherein the plurality of logic gates are implemented with firmware.

14. (Original) The encoder of claim 1, wherein the encoder is implemented with software that is executed with a processor.

15. (Currently Amended) The encoder of claim 1, wherein the ~~variable~~ time delay is implemented by a reference code of A=212124 octal and B=1202401 octal.

16. (Currently Amended) An interleaved generalized convolutional encoder, comprising:

~~(a)~~ a ~~variable~~ time delay element having a delay value M, where M is configurable at run-time to a first value;

~~(b)~~ a switch;

~~(c)~~ a plurality of convolutional encoders being capable of receiving a data input, the data input being a portion of ~~a data symbol~~ one of a stream of data symbols, wherein the data input is received by the switch and directed to one of the plurality of convolutional encoders based on the ~~variable~~ time delay element;

~~(d)~~ the plurality of convolutional encoders being capable of storing a plurality of prior data inputs, the prior data inputs for any one of the convolutional encoders being a portion of each of a plurality of prior data symbols directed to the one of the convolutional encoders, the plurality of prior data inputs being subjected to a unit time delay; and

~~(e)~~ a plurality of logic calculators associated with each of the plurality of convolutional encoders,

~~(i) a portion of the plurality of logic calculators being capable of receiving a coefficient input,~~

~~(ii)~~ the plurality of logic calculators ~~including at least one final logic calculator, the at least one final logic calculator being capable of producing an output~~,

~~(A)~~ ——the plurality of logic calculators generating an output being based on the data input, the plurality of prior data inputs, the plurality of logic calculators, ~~the coefficient input,~~ and the ~~variable~~ time delay element.

17. (Original) The encoder of claim 16, wherein the data input is a portion of a PAM symbol.

18. (Original) The encoder of claim 16, wherein the data input is processed by a serial to parallel converter prior to entering the switch.

19. (Original) The encoder of claim 16, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

20. (Original) The encoder of claim 16, wherein a receiver sets the delay associated with the variable time delay element.

21. (Currently Amended) The encoder of claim 16, wherein a receiver dynamically sets the delay associated with the ~~variable~~ time delay element.

22. (Currently Amended) The encoder of claim 21, wherein the delay associated with the ~~variable~~ time delay element is based on the quality of a transmission path between a transmitter and the receiver.

23. (Currently Amended) The encoder of claim 21, wherein the delay associated with the ~~variable~~ time delay element is based on noise affecting the transmission of data between a DTE and the receiver.

24. (Currently Amended) The encoder of claim 16, wherein the delay associated with the ~~variable~~ time delay is three bauds.

25. (Original) The encoder of claim 16, wherein the plurality of logic calculators includes a plurality of binary exclusive-OR gates and a plurality of binary AND gates.

26. (Original) The encoder of claim 16, wherein the output is processed by a mapper after exiting the encoder.

27. (Original) The encoder of claim 16, wherein the plurality of logic gates are implemented with firmware.

28. (Original) The encoder of claim 16, wherein the encoding system is implemented with software that is executed with a processor.

29-30. (Cancelled)

31. (Currently Amended) A system for encoding information, comprising:

~~(a)~~ first means for receiving a data input, the data input being a portion of ~~a data symbol~~ one of a stream of data symbols;

~~(b)~~ second means for ~~variably~~ delaying a plurality of prior data inputs for a time unit M, where M is configurable at run-time to a first value, the plurality of prior data inputs being a portion of each of a plurality of prior data symbols;

~~(c)~~ third means for storing the ~~variably~~ delayed plurality of inputs;

~~(d)~~ fourth means for performing logic calculations; and

~~(e) fifth means for receiving a coefficient input; and~~

~~(f)~~ ——fifth ~~sixth~~ means for producing an output, wherein the output is based on the operation of the first means, the second means, the third means, and the fourth means~~, and the fifth means~~.

32. (Original) The system of claim 31, wherein the data input is a portion of a PAM symbol.

33. (Original) The system of claim 31, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

34. (Currently Amended) The system of claim 31, wherein a receiver determines the value of the ~~variably~~ delay of the means for variably delaying a plurality of inputs.

35. (Currently Amended) The system of claim 31, wherein a receiver dynamically determines the value of the ~~variably~~ delay of the means for variably delaying a plurality of inputs.

36. (Currently Amended) The system of claim 35, wherein a value of the ~~variably~~ delay is based on the quality of a transmission path between a transmitter and the receiver.

37. (Currently Amended) The system of claim 35, wherein a value of the ~~variably~~ delay is based on noise affecting the transmission of data between a DTE and the receiver.

38. (Currently Amended) The system of claim 31, wherein a value of the ~~variably~~ delay is three bauds.

39-49. (Cancelled)

50. (Currently Amended) A computer readable medium for encoding information, comprising:

~~(a)~~ logic for receiving a data input, the data input being a portion of ~~a data symbol~~ one of a stream of data symbols;

~~(b)~~ logic for ~~variably~~ delaying a plurality of prior data inputs for a time unit M, where M is configurable at run-time to a first value, the plurality of prior data inputs being a portion of each of a plurality of prior data symbols;

~~(c)~~ logic for storing the ~~variably~~ delayed plurality of inputs;

~~(d)~~ logic for performing logic calculations; and

~~(e) fifth means for receiving a coefficient input; and~~

(f) logic for producing an output, the output being based on the operation of the logic for receiving a data input, the logic for ~~variably~~ delaying a plurality of prior data inputs, the logic for storing the ~~variably~~ delayed plurality of prior data inputs, and the logic for performing logic calculations, ~~and the logic for receiving coefficient input~~.

51. (Original) The system of claim 50, wherein the data input is a portion of a PAM symbol.

52. (Original) The system of claim 50, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

53. (Currently Amended) The system of claim 50, wherein a receiver determines the value of the ~~variable~~ delay of the logic for variably delaying a plurality of prior data inputs.

54. (Currently Amended) The system of claim 50, wherein a receiver dynamically determines the value of the ~~variable~~ delay of the logic for variably delaying a plurality of prior data inputs.

55. (Currently Amended) The system of claim 54, wherein a value of the ~~variable~~ delay is based on the quality of a transmission path between a transmitter and the receiver.

56. (Currently Amended) The system of claim 54, wherein a value of the ~~variable~~ delay is based on noise affecting the transmission of data between a DTE and the receiver.

57. (Currently Amended) The system of claim 50, wherein a value of the ~~variable~~ delay is three bauds.

58-77. (Cancelled)

78-89. (Cancelled)

90. (New) The encoder of claim 1, where M has the same first value for successive symbols in the stream of data symbols unless reconfigured to a second value.

91. (New) The encoder of claim 16, where M has the same first value for successive symbols in the stream of data symbols unless reconfigured to a second value.

92. (New) The system of claim 31, where M has the same first value for successive symbols in the stream of data symbols unless reconfigured to a second value.

93. (New) The computer readable medium of claim 50, where M has the same first value for successive symbols in the stream of data symbols unless reconfigured to a second value.